CLAIM AMENDMENTS:

Claim 1 (Previously Presented): A method of fabricating a semiconductor device having trenches, comprising:

a mask forming step comprised of sequentially forming a first insulating film and a second insulating film on a semiconductor substrate, followed by forming a mask for forming trenches on the second insulating film by patterning so as to expose a surface area of the second insulating film corresponding to each trench formed on the semiconductor substrate;

a trench forming step comprised of etching a portion extending from the surface area of the exposed second insulating film to an in-depth part of the semiconductor substrate using the mask for forming trenches, thereby forming the trenches on the semiconductor substrate;

a depositing step comprised of removing the mask for forming trenches, followed by depositing a third insulating film by filling a third insulating film into each trench up to the height to cover the second insulating film;

a second oxide film forming step performed through the third insulating film and after said depositing a third insulating film, and being comprised of subjecting the semiconductor substrate at a cornered portion of each trench to thermal oxidation, thereby forming a second oxide film, wherein said second oxide film forming step includes supplying oxygen from an upper side of the third insulating film so that the oxygen is diffused into the third insulating film, and so that an oxidative reaction starts at the cornered portion;

a planarizing step performed after said second oxide film forming step, and comprising polishing and planarizing the third insulating film so as to expose the second insulating film; and

an element isolation portion forming step comprised of removing the second insulating film and the first insulating film, followed by etching the third insulating film such that a part of the third insulating film remains inside each trench, thereby forming an element isolating portion.

Claims 2 and 3 (Canceled).

Claim 4 (Original): The method of fabricating a semiconductor device having trenches according to claim 1, wherein the first insulating film is a silicon oxide film and the second insulating film is a silicon nitride film.

Claim 5 (Original): The method of fabricating a semiconductor device having trenches according to claim 1, wherein the third insulating film is a silicon oxide film.

Claim 6 (Original): The method of fabricating a semiconductor device having trenches according to claim 4, wherein the third insulating film is a silicon oxide film.

Claim 7 (Original): The method of fabricating a semiconductor device having trenches according to claim 1, wherein the third insulating film is formed by an HDP-CVD method.

Claim 8 (Original): The method of fabricating a semiconductor device having trenches according to claim 5, wherein the third insulating film is formed by an HDP-CVD method.

Claim 9 (Original): The method of fabricating a semiconductor device having trenches according to claim 6, wherein the third insulating film is formed by an HDP-CVD method.

Claim 10 (Canceled).

Claim 11 (New): The method of fabricating a semiconductor device having trenches according to claim 1, wherein the oxygen is supplied during said second oxide forming step while subjecting the semiconductor substrate to the thermal oxidation.

Claim 12 (New): The method of fabricating a semiconductor device having trenches according to claim 11, wherein the oxygen that is supplied during said second oxide forming step is dry oxygen.

Claim 13 (New): The method of fabricating a semiconductor device having trenches according to claim 12, wherein the thermal oxidation is performed at a temperature of about 1100°C.

Claim 14 (New): The method of fabricating a semiconductor device having trenches according to claim 1, wherein the oxygen that is supplied during said second oxide forming step is dry oxygen.

Claim 15 (New): The method of fabricating a semiconductor device having trenches according to claim 1, wherein the thermal oxidation is performed at a temperature of about 1100°C.